MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023

EEE1026 – ELECTRONICS II

(All Sections / Groups)

10 JULY 2023
9.00 a.m – 11.00 a.m
(2 Hours)

INSTRUCTION TO STUDENT

1. This Question paper consists of **9** pages including cover page with **4** Questions only.

2. Attempt **ALL** questions. All questions carry different marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

Question 1

(a) Figure Q1(a) below shows a n-channel Junction Field Effect Transistor (JFET) biased with a voltage divider circuit. The JFET has a supply voltage $V_{DD} = 20$ V and the maximum drain-source current $I_{DSS} = 9$ mA. It is given that the voltage at the drain terminal, V_D is 9 V.

(i) Calculate the gate voltage, V_G. [2 marks]

(ii) Determine the drain current I_D. [2 marks]

(iii) Calculate the source voltage, V_S. [2 marks]

(iv) Calculate the pinch-off voltage, V_P. [4 marks]

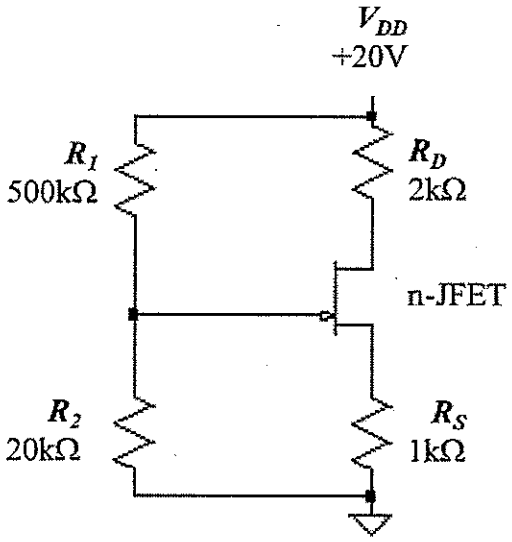

Figure Q1(a)

Continued...

Question 1

(b) Figure Q1(b) shows an amplifier circuit with an *n*-channel JFET. Given that supply voltage V_{DD} = 20 V, pinch off voltage V_p = -6 V, maximum drain-source current I_{DSS} = 10 mA, internal resistance r_d = 30 kΩ, and V_{GSQ} = -2 V.

(i) Draw a small-signal equivalent circuit with a transistor model for the network shown in Figure Q1(b). [5 marks]

(ii) Determine the transconductance, g_m. [3 marks]

(iii) Determine the input impedance, Z_i. [2 marks]

(iv) Determine the output impedance, Z_o without r_d. [2 marks]

(v) Determine the voltage gain, A_V without r_d. [3 marks]

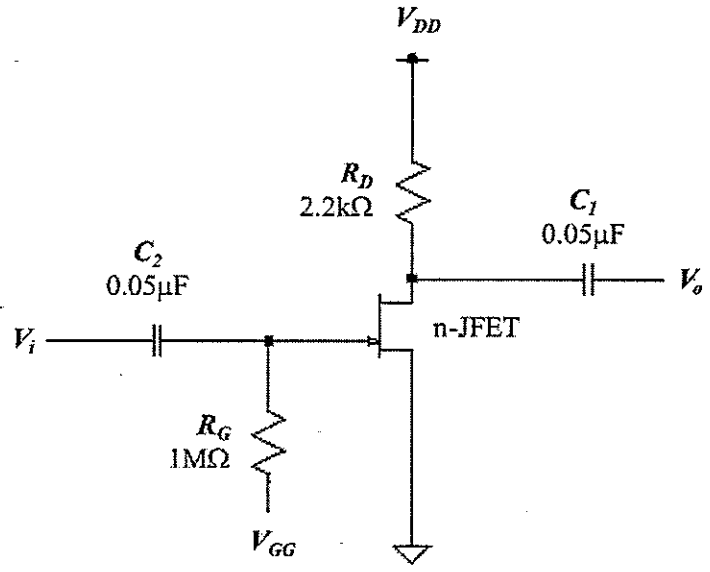

Figure Q1(b)

Continued...

Question 2

(a) An operational amplifier (op-amp) is shown in Figure Q2(a). Given R_i = 10 kΩ, R_f = 20 kΩ and DC supply voltages ±V = ±10 V. Assume that the op-amp output has a loss of 1V.

(i) Determine the upper trigger point (*UTP*) and lower trigger point (*LTP*) values. [4 marks]

(ii) Given that the input V_{in} is a sinusoidal signal with a peak-to-peak voltage, V_{PP} = 20 V, sketch the output voltage waveform with respect to its input waveform. [8 marks]

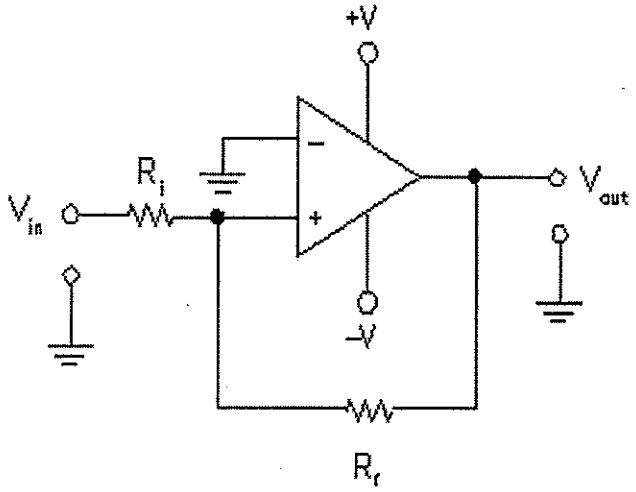

Figure Q2(a)

Continued...

Question 2

(b) An astable multivibrator using a 555 timer integrated circuit (IC), as shown in Figure Q2(b), has $V_{CC} = 10$ V, $R_A = 5$ kΩ, $R_B = 2$ kΩ and $C_1 = 0.022$ μF.

(i) Describe the operation of the multivibrator, assuming that the output from the flip-flop (FF) is low.

[5 marks]

(ii) Determine the values of pulse width (T_1) and space width (T_2).

[4 marks]

(iii) Calculate the free running frequency (f_0) and the duty cycle (D).

[4 marks]

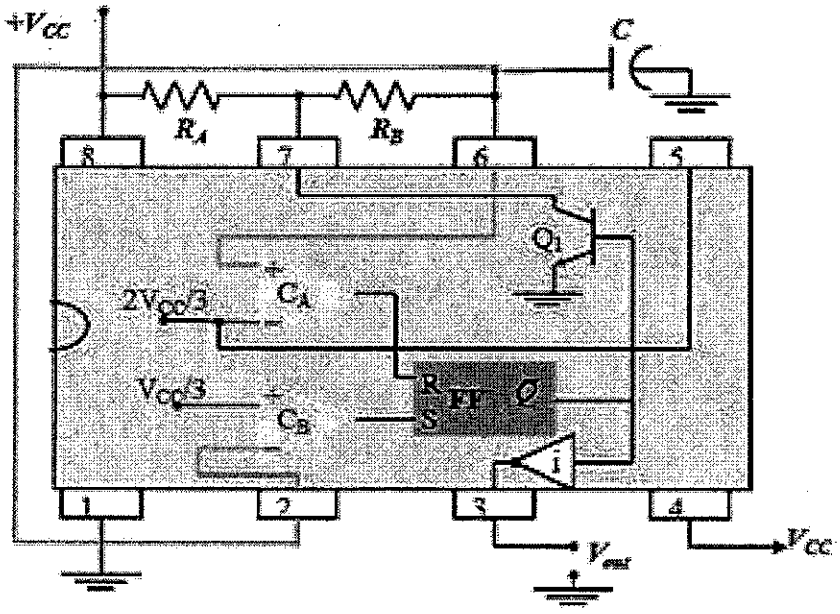

Figure Q2(b)

Continued...

Question 3

(a) Figure Q3(a) shows a common-source Junction Field Effect Transistor (JFET) amplifier circuit.

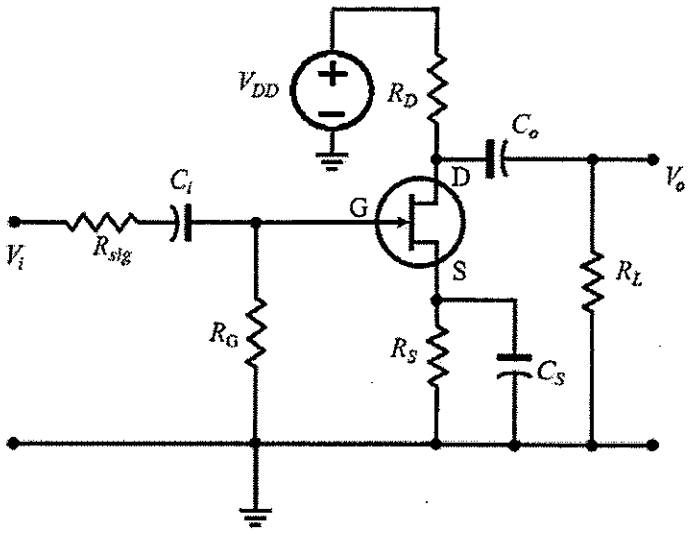

Figure Q3(a)

(i) Draw the high-frequency small-signal equivalent circuit of the amplifier. Next, briefly explain the reason for the addition of parasitic capacitances in the transistor model.

[6 marks]

(ii) Applying the Miller theorem to the circuit in Question 3(a)(i), draw its small-signal equivalent circuit. State the Miller effect equations to represent the effective capacitances at the input and output circuits.

[5 marks]

Continued...

Question 3

(b) The amplifier circuit of Figure Q3(b) is analysed for its low-frequency characteristics.

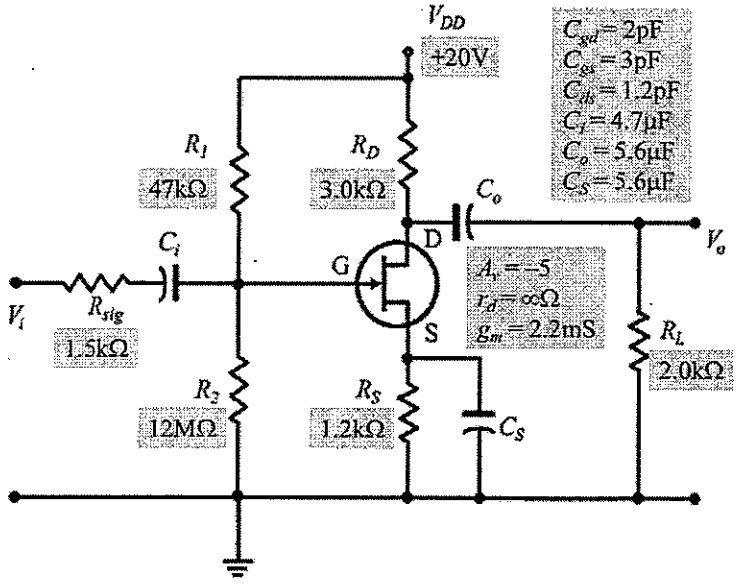

Figure Q3(b)

(i) Determine f_{Lci}, f_{Lco} and f_{Lcs}, which are the frequencies associated with the coupling capacitors C_i and C_o, and the by-pass capacitor C_S, respectively.

[9 marks]

(ii) Sketch the low-frequency response of the amplifier, clearly indicating the asymptotes, and the frequencies f_{Lci}, f_{Lco} and f_{Lcs}.

[5 marks]

Continued...

Question 4

(a) The push-pull circuit of Class-B amplifier can deliver higher power efficiency compared to Class-A amplifier.

(i) Draw the circuit configuration of Class-B amplifier with its load, bias resistors and coupling capacitors.

[4 marks]

(ii) Using block diagram representation of the Class-B amplifier, describe how such an amplifier achieves its full 360° input signal operation. Next, draw the corresponding waveform of its output with respect to the input signal.

[9 marks]

(b) A Class-A power amplifier is shown in Figure Q4(b). Using the approximation method, determine the following:

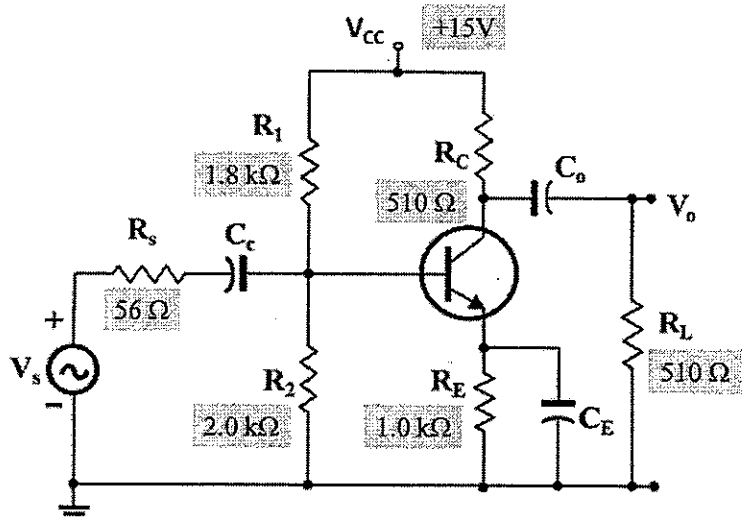

Figure Q4(b)

(i) the emitter voltage, V_E, and the emitter current, I_E ,

[3 marks]

(ii) the quiescent collector-to-emitter voltage, V_{CEQ} and the equivalent load resistance, r_c ,

[3 marks]

(iii) $i_{C(sat)}$ and $v_{CE(cutoff)}$, and,

[4 marks]

(iv) draw the AC load line diagram.

[2 marks]

Continued...

Appendix A

List of Equations

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(OFF)}}\right)^2$$

$$UTP = \frac{R_2}{R_1+R_2}V_{out+} \qquad LTP = \frac{R_2}{R_1+R_2}V_{out-}$$

$$\text{Tilt\%(P)} = \frac{V-V'}{V}, \quad f_L = \frac{P}{\pi}f_s$$

$$PW = 0.693\ (R_A + R_B)\ C_1\ ,\ SW = 0.693\ R_B C_1$$

$$f = \frac{1.44}{(R_A+2R_B)C_1}$$

End of paper